

HIPEX

Release Notes

03/01/12

RELEASE NOTES

VERSION 3.4.24

ALTERATIONS AND ENHANCEMENTS

- Baseline Release
- Improve optional exclusion of gate width from computing of source/drain perimeter
- Reduce resistance extraction sensitivity to contact/via sizes

VERSION 3.4.23

NEW FEATURES

- LAYOUT_TEXT command to provide virtual assignment of net names
- Rapid parameter calculator in generic device extraction

ALTERATIONS AND ENHANCEMENTS

- Eliminate redundant resistors on device pins in HIPEX-R
- Improve shape decomposition in resistance extraction introducing polygon purification utility
- Introduce more precise method of resistance extraction for nets with dangled branches
- Improve hierarchical extraction mode for instance arrays

VERSION 3.4.22

NEW FEATURES

- Introduce faster and more precise methods into resistance extraction for complex, regular patterned shapes that occurred in LCD layouts
- Enable parasitic resistance extraction with possibility of executing user-defined scripts written either in LISA or JavaScript
- Enable CPX OVERLAP command with custom scripting in LISA and JavaScript offering an extended set of measurements

- Add new option HIPEX_SOFTCHECK_WARNINGS_AS_ERRORS for netlist extraction

ALTERATIONS AND ENHANCEMENTS

- Improve processing of wire bends with changing of conductor width in HIPEX-R
- Enhance the treatment of port labels in HIPEX-R to reduce sensitivity to the width of encapsulating conductor
- Improve extraction of parallel metals filled with via contacts
- Amend shape decomposition engine in HIPEX-R to control connectivity and prevent the fractionating of parasitic resistive network

VERSION 3.4.15

NEW FEATURES

- Adjust DSPF output to comply with Static Timing Analysis requirements:
 - remove the *|NET section for the power net
 - include parasitic capacitors from the power net to other (ordinary) nets into the *|NET sections created for those nets
- Control the inclusion of dangling nets into DSPF netlist by CPX_EXTRACT_DANGLES variable
- Introduce Distribution Modes ACCURATE and THRIFTY to control the method for generation of RC netlist from extracted R and C parasitic networks
- Change the extraction of MOSFET with connected source/drain. Assign the drain and source terminal with the same net name if the source and drain regions are drawn together as a single polygonal region.
- Add SHIELD_FACTOR parameter to Area Capacitor specification. If the shape from the layer enumerated within INSIDE_LAYERS group separates the plates of area capacitor, then resulting capacitance is scaled with SHIELD_FACTOR value
- Enable restriction on maximum length of lines for HIPEX-generated netlists with use of the variable NETLIST_LINE_LENGTH; SPICE, DSPF, and SPEF formats affected

ALTERATIONS AND ENHANCEMENTS

- Correct DSPF output to avoid instances of empty sub-circuits
- Prevent incorrect back-annotation for the case of different hierarchical structures of schematic and extracted netlists

VERSION 3.4.8

NEW FEATURES

- Allow HIPEX_COMMENT_MODEL variable to comment both device models and the .END statement in the output SPICE netlist

ALTERATIONS AND ENHANCEMENTS

- Increase speed and accuracy of resistance calculation for selected terminal configurations
- Prevent incorrect appearance of synonyms for pin names in generic devices