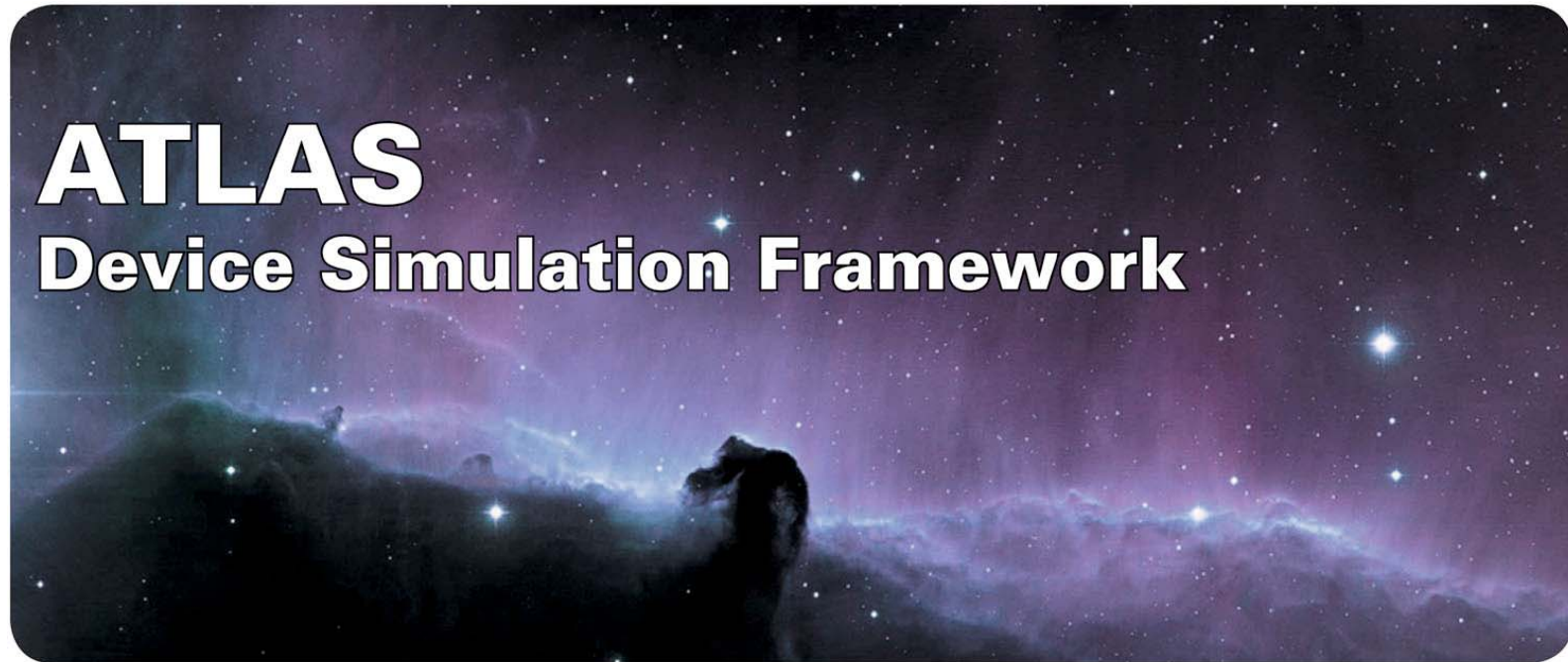


Tuning Parameters for Accurate MOSFET Simulation



SILVACO



Basic Simulation Guidelines

- For accurate simulation of MOSFETs, 90% of the effort should be invested in achieving an accurate PROCESS simulation while only 10% of the time should be spent fine tuning Device simulation
- Device physics better characterized than new process physics (90%/10% rule)
- Device physics doesn't change but new processes continue to evolve



Basic Guidelines (con't)

- If the device simulation is way off from the measured data, most probably you've done something wrong in the PROCESS simulation
- Exception: Inappropriate gridding
- Golden Rule: DO NOT CHANGE WELL KNOWN COEFFICIENTS!

eg. DIX.0, DIP.0 & DIM.0



What Measured Data are Needed to Correctly Calibrate the Models?

- Two types of required measured data:-
 - Essential data for Process Modeling
 - Verification data (I-V curves etc)

(this is data NOT used in process models to check the predictive nature of the simulation)



Process Modeling Data

- THE PROCESS FLOW !
- V_t versus Gate Length (Minimum Geometry up to 20 μm Gate length)
- Accurate gate oxide thickness (Care! quantum C-V effects and/or poly depletion)
- Accurate spacer width/profile (preferably SEM micrographs)
- SIMS profiles



Why do I need Data for 20 μ m Gate Lengths ?

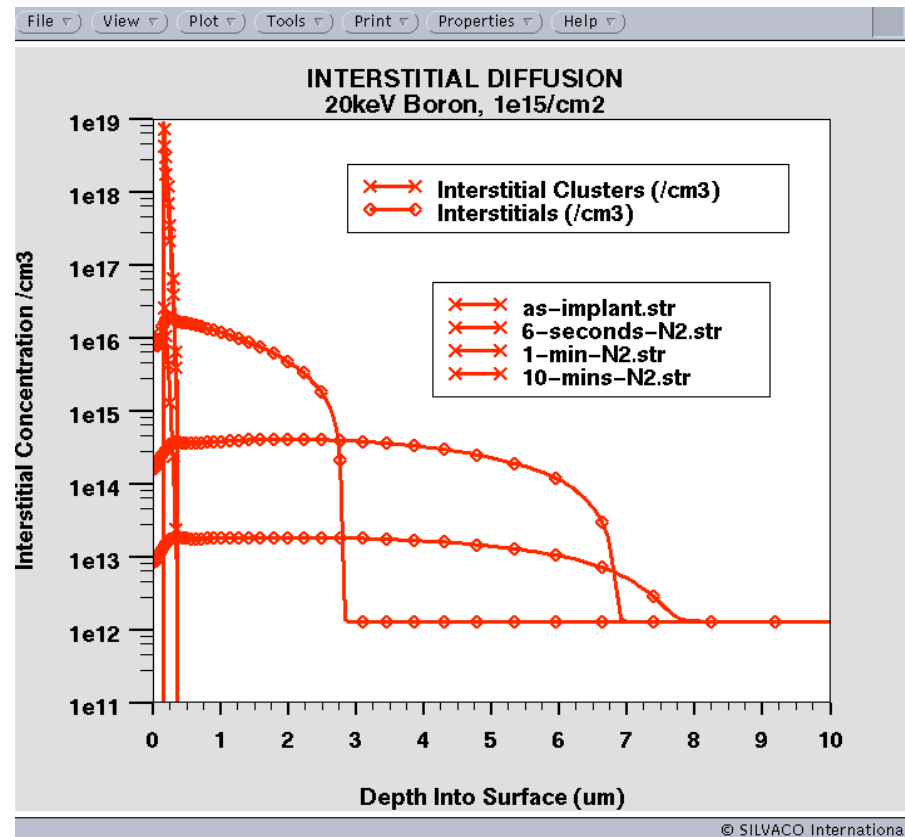
- Interstitials greatly enhance diffusion with a resultant strong influence on V_t
- Interstitials generated by implantation, oxidation and silicidation typically travel 10 μ m along the surface and up to 20 μ m deep

(surface defect recombination >> bulk defect recombination)

- The diffusion length of interstitials is much longer than 1 μ m (see page 7). Therefore, if simulated substrate depth is less than the diffusion length then the simulated interstitial concentration will be artificially high. This will result on “excessive” boron diffusion (see page 8)



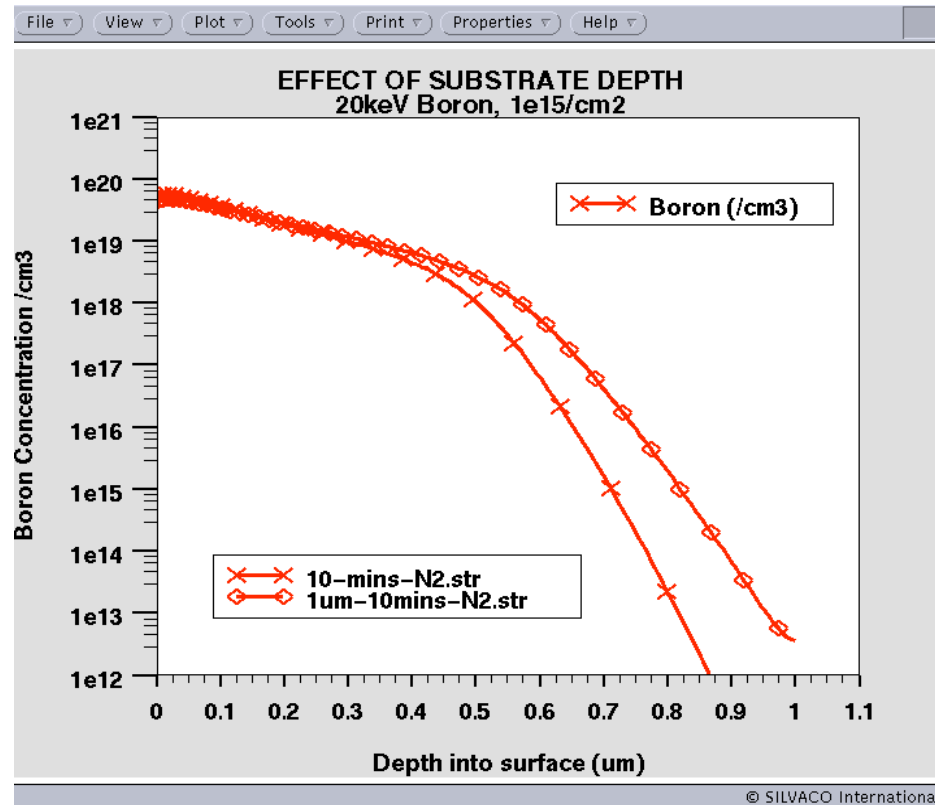
Interstitial Diffusion



The diffusion of interstitial damage during post implantation anneals.



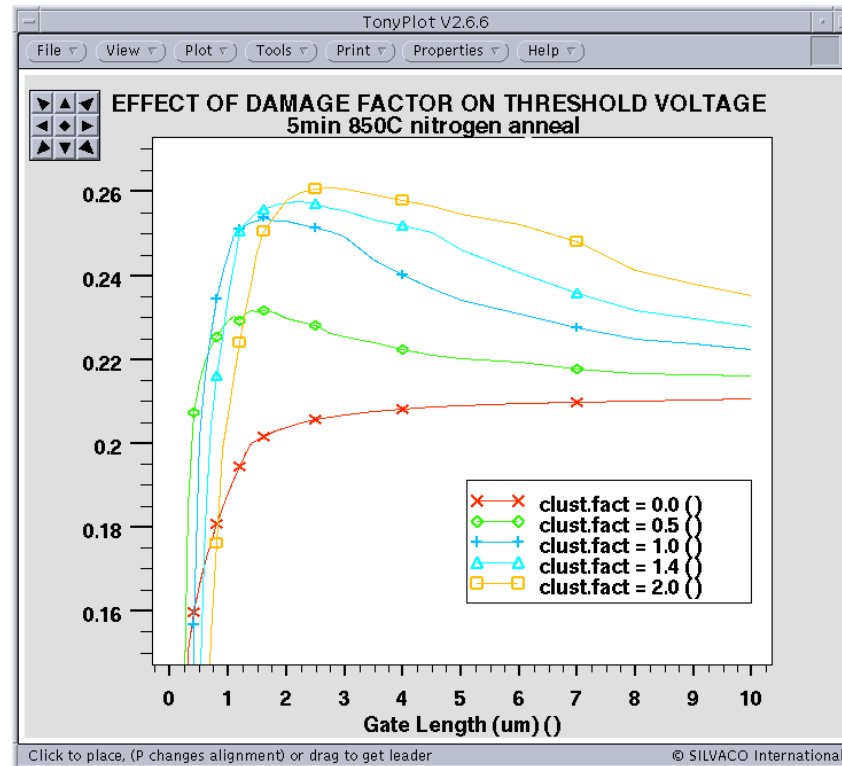
Effect of Substrate Depth



The effect on the boron depth profile of reducing the simulated substrate depth from $20\mu\text{m}$ to $1\mu\text{m}$



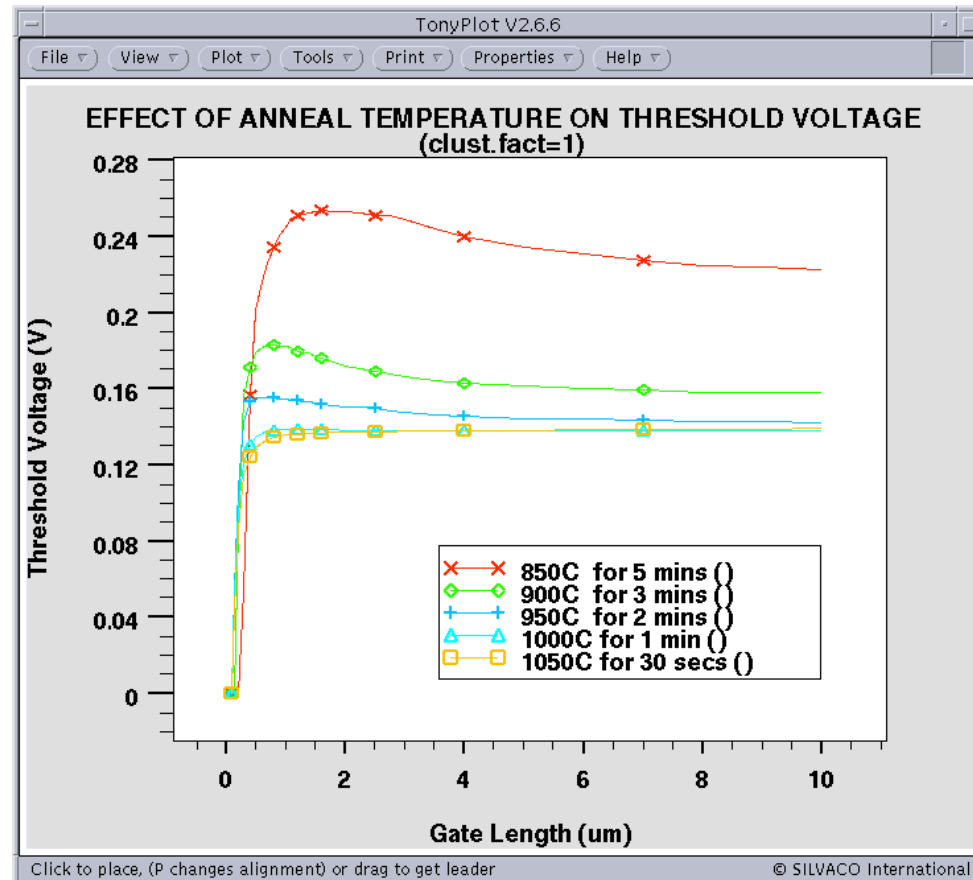
Effect of Damage Factor on Threshold Voltage



Graph of V_t versus gate length for (i) No interstitial injection (ii) Realistic model (showing asymptotic behavior at $20\mu\text{m}$)



Effect of Anneal Temperature on Threshold Voltage





The Importance of Correctly Modeling Interstitials

- Interstitial enhanced diffusion important for channel implant during Gate Oxidation(V_t is very sensitive to this diffusion)
 - Empirical evidence indicates:
for a given oxide thickness the total number of interstitials injected is greater for wet compared to dry therefore greater total diffusion possible

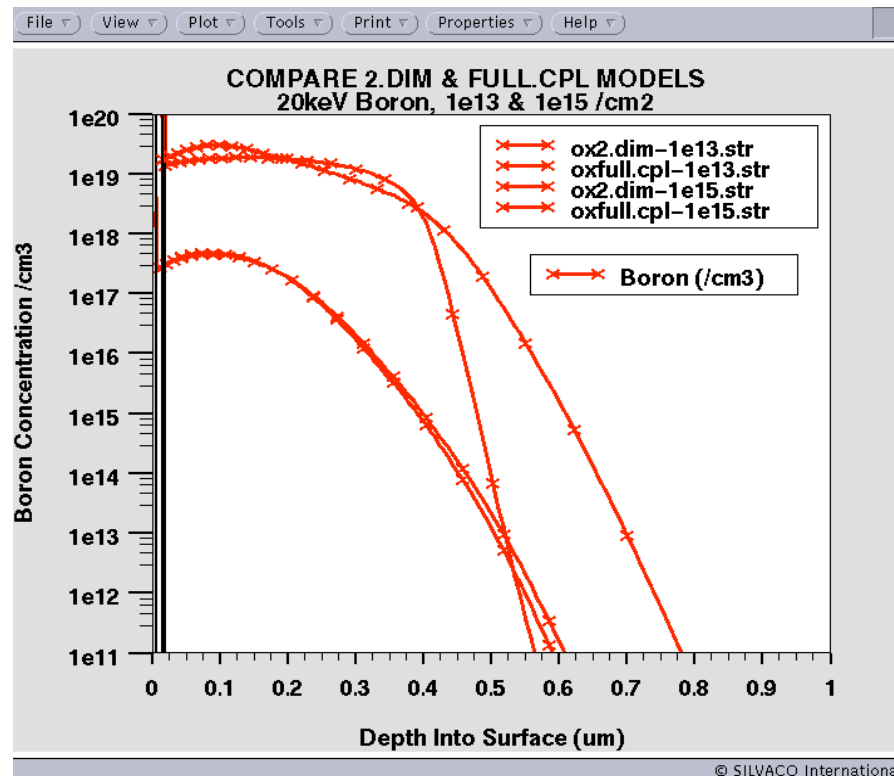


Oxidation & Diffusion Models

- FERMI model - basic^[1]
- TWO.DIM model - intermediate^[2]
- FULL.CPL model- advanced^[3]
 - [1] - constant interstitial concentration, OK for non implanted material
 - [2] - OK for implants $< 1 \times 10^{13} / \text{cm}^2$
 - [3] - required for implants $> 1 \times 10^{13} / \text{cm}^3$



Comparison of TWO.DIM and FULL.CPL Models



Comparison between TWO.DIM and FULL.CPL models for low dose ($1 \times 10^{13} / \text{cm}^2$) and high dose ($1 \times 10^{15} / \text{cm}^2$) implants

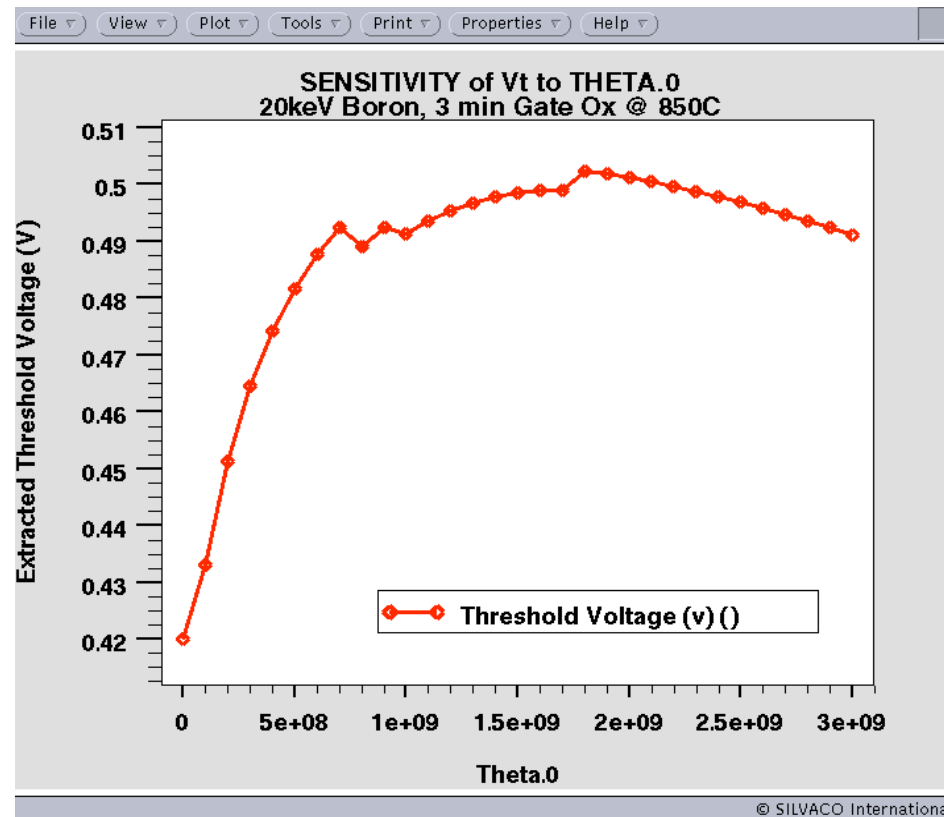


Tuning Diffusion During Gate Oxidation

- Use MEASURED long channel (20 μ m) V_t
 - Tune THETA.0 at center channel in 1D
 - THETA.0 controls interstitials injection at oxide/silicon boundary during oxidation. It is specified in the INTERSTITIAL statement
 - Fine tune THETA.0 using 2D



Sensitivity of V_t to Θ_0



The Effects of Θ_0 on V_t (Note the “EXTRACT” auto-gridding error of approximately 0.002 volts if the default grid setting is used)



For High Dose LDD & Source/Drain Implants

- $\langle 311 \rangle$ CLUSTER DAMAGE model MUST be used
- Tune `CLUST.FACT` to obtain the correct peak in the RSCE (V_t versus gate length plot)
- The `CLUSTER.DAM` model effectively causes a time release of interstitials.
- Tune spacer width to determine the rate of V_t falloff for very short gate lengths (SCE)
- BCA implant model is preferable for all sensitive implant steps



For LDD & Source/Drain RTA Activation

- The `CLUSTER.DAM FULL.CPL` models **MUST** be used initially or for at least twice the 95% decay time (see following table)
- Tune `KSURF.0` to obtain the correct long channel fall off in V_t versus gate length
- The `FULL.CPL` model also takes account of dopant-defect pair formation



Transient Enhanced Diffusion

Anneal Temperature	Time of Complete 95% of TED
600	390 hours
700	3.3 hours
750	30 minutes
800	3.7 minutes
850	43 seconds
900	8.3 seconds
950	1.9 seconds
1000	0.48 seconds
1050	0.13 seconds

Simulated length enhanced diffusion versus anneal temperature based on <311> cluster decay kinetics, for a 50eV, $1e14 \text{ cm}^{-3}$ implant.



p-Channel RSCE

- For buried p-channel devices, high angle implants usually cause RSCE
- Boron source/drain regions absorb interstitials rather than inject them so do NOT use the “cluster.dam” model for high dose boron implants. Unset the “cluster.dam” model using “cluster.dam=f” if it has been set previously in the input file



Device Simulation (Verification)

- Remember:
 - If the process modeling was accurate...the electrical characteristics should be too.
 - If not, you have done something wrong with the PROCESS or the GRID.



The Grid! (or Mesh)

- A suitable grid for process simulation may not be suitable for device simulation
- In general, minimize the number of mesh points
Solution time $\gg k^*(\text{mesh points})^{2-3}$
- BUT... too few mesh points can take LONGER since each solution takes longer to converge. You cannot beat experience here
- 10Å mesh in inversion regions. Concentrate mesh at metalurgic junctions



Device Modeling Data

- C-V data
- Contact resistance measurements
- I_d - V_d | V_g curves
- I_d - V_g | V_b curves
- I_d - V_d for $V_g=0$ (breakdown characteristic)

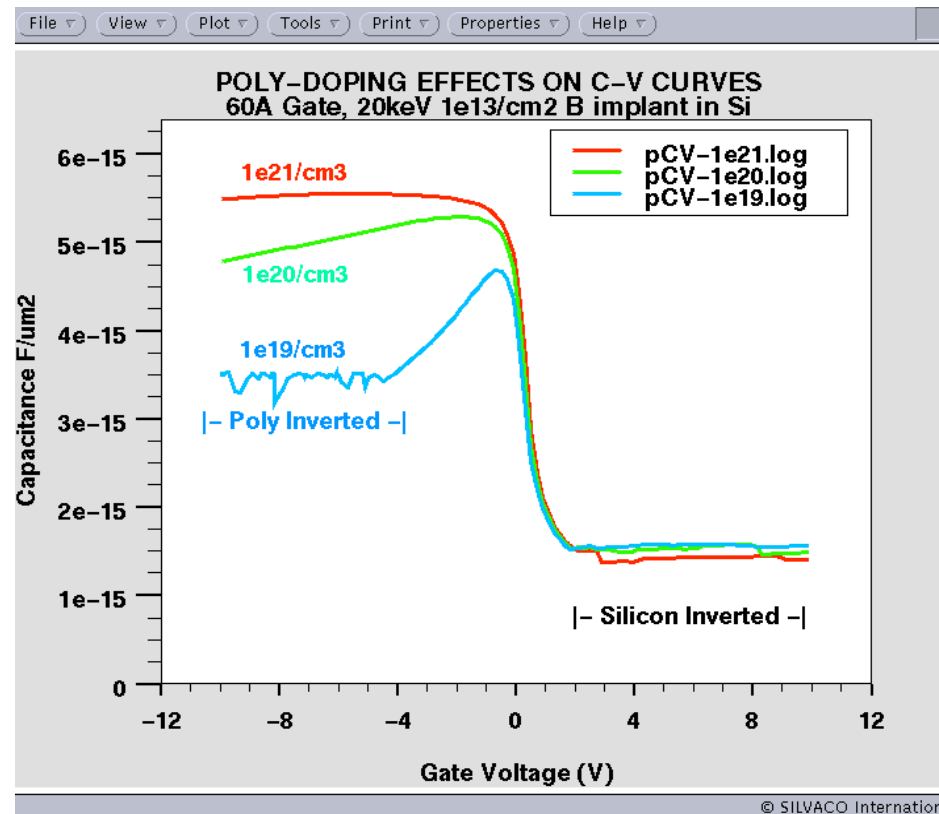


Gate Structures

- Look for C-V accumulation anomalies
 - If anomalous, poly dopant has been consumed by silicide giving non ideal workfunction
- Use a separate metal contact for simulation or adjust poly workfunctions
- Typical values:-
 - 4.17 for in situ N++ poly doping
 - 4.3 to 4.4 for implanted P+ compensated



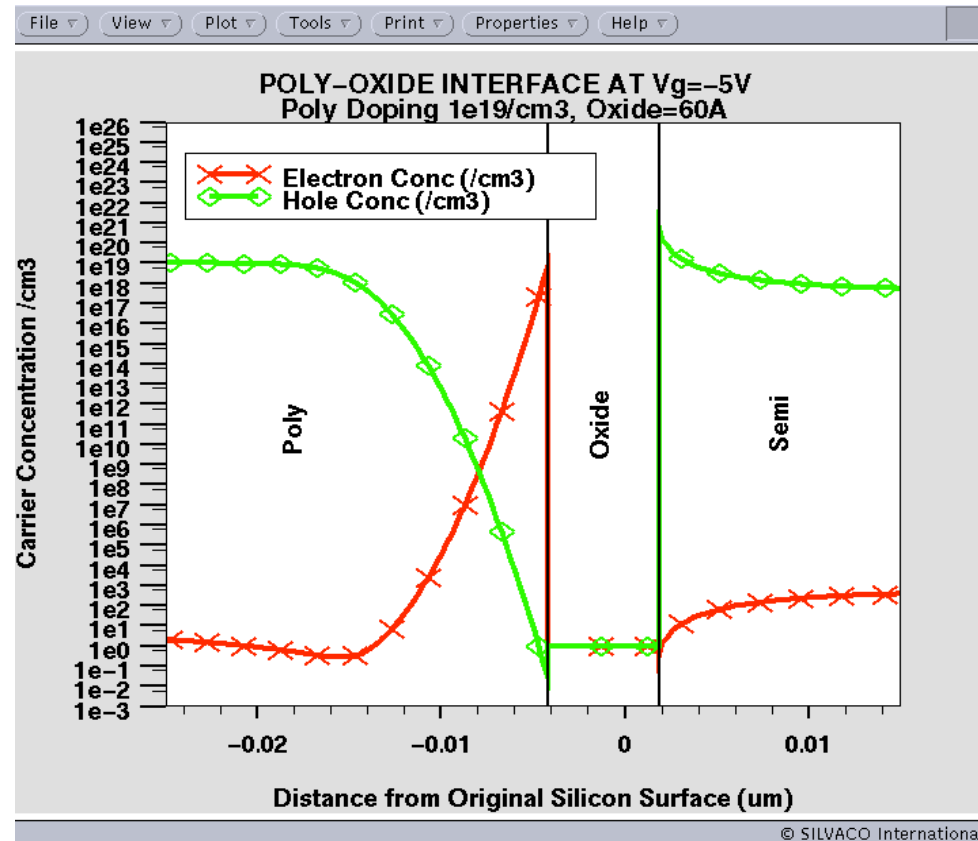
Poly-Doping Effects on C-V Curves



The Effects of Poly-Doping on the Accumulation Region of a Standard High Frequency C-V Plot.



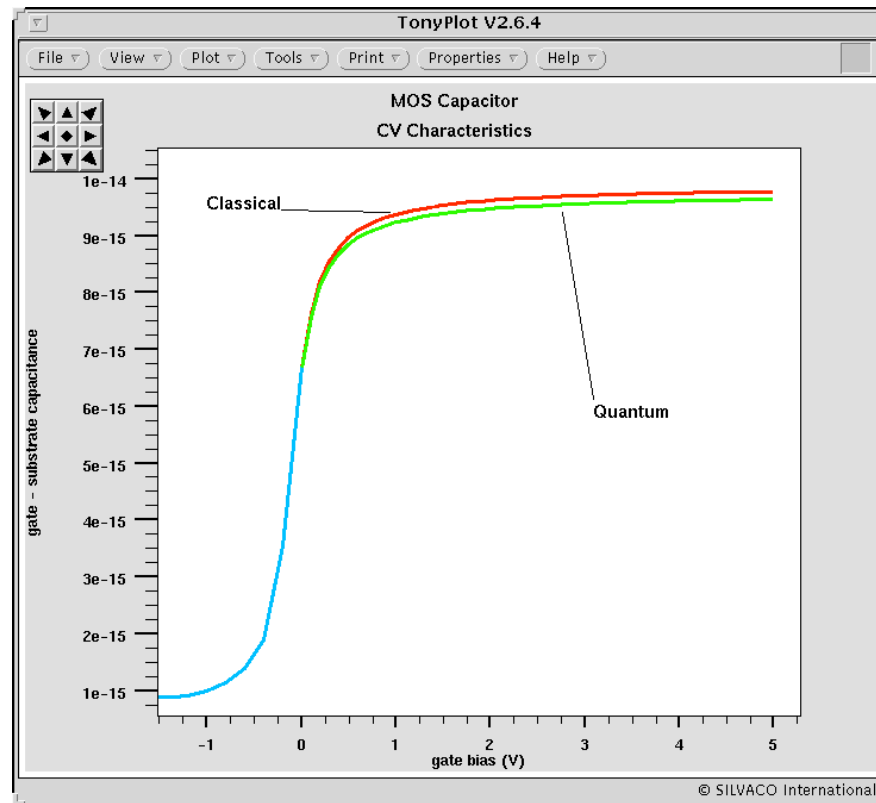
Poly-Oxide Interface



Inversion at the Poly-Oxide Interface for a Poly Doping of $1e^{19}/cm^3$ and a Gate Bias of -5 Volts



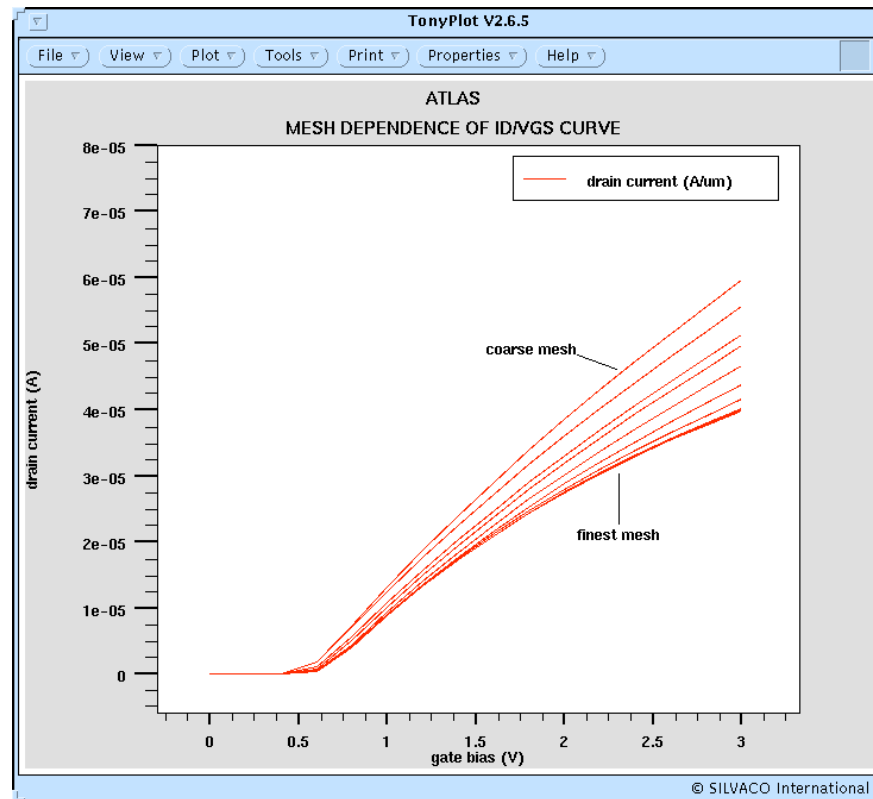
MOS Capacitor CV Characteristics



Graph showing differences between the calculated accumulation capacitance MOS of a capacitor using classical and quantum moment calculations



Mesh Dependence of ID/VGS Curves



Graph showing effect of increased I_d for wide grid spacing showing the requirement for a grid density for the inversion region of 10\AA typically



Parasitic Resistance

- Source and drain parasitic resistance each given by:-

$$R_{S \text{ or } D} = \frac{R \times W}{N}$$

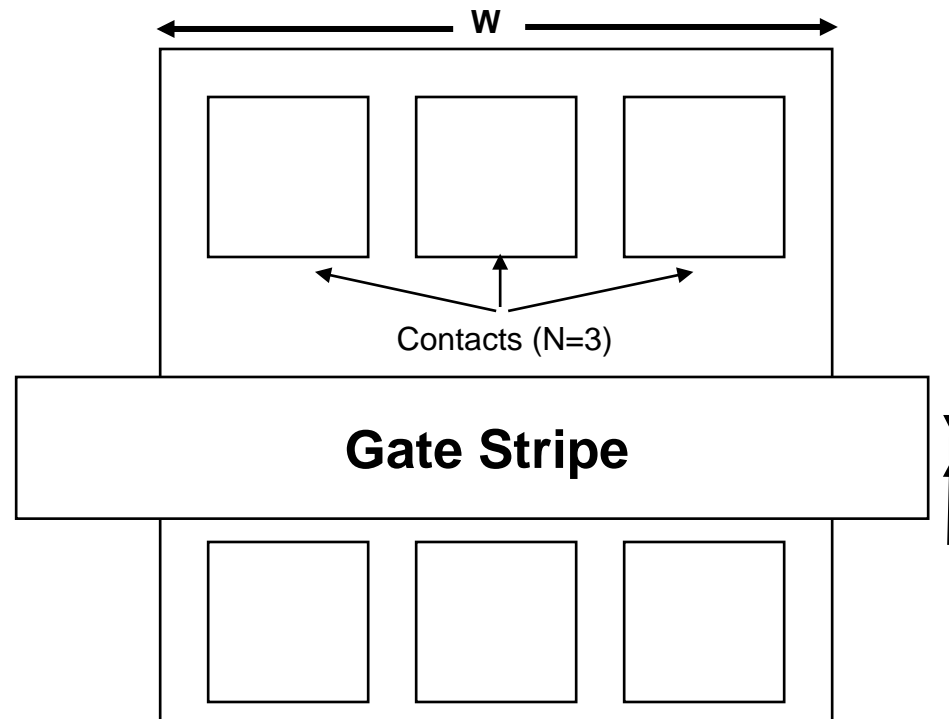
Where:- R = the resistance per via

W = the device width

N = the number of bias in each contact



Calculation of Contact Resistance



Schematic diagram showing how contact resistance should be calculated, for a device with 3 bias per contact.



Check the Model

- Use data NOT used for tuning to check the predictability of the model
- Good example:- I-V curves with substrate bias



MOSFET Tuning Simulation Summary

- (i) Measure V_t versus gate length to $20\mu\text{m}$
 - (ii) Accurately measure gate oxide thickness
 - (iii) Measure spacer thickness and profile
 - (iv) Ensure the substrate is at least $25\mu\text{m}$ deep
- } **Physical device measurements**
- (v) Use *TonyPlot* to ensure sufficient grid for channel implant
- (vi) Tune the gate oxide thickness (thin gates)
 - (vii) Tune Theta0 to V_t using $20\mu\text{m}$ gate length (1D)
 - (viii) Fine tune Theta0 using $20\mu\text{m}$ gate length (2D)
- } **Use FULL.CPL Model in most cases**
- (ix) Tune spacer oxide to obtain correct dimensions/profile



MOSFET Tuning Simulation Summary (con't)

- (x) Use <311> CLUSTER.DAM model for arsenic LDD & S/D implants but not for boron implants
- (xi) Use FULL.CPL model for RTA activation
- (xiv) Tune CLUST.FACT to obtain correct peak value in V_t
- (xv) Tune spacer width to obtain correct true SCE rolloff
(also important for peak V_t in buried p-channel RSCE)
- (xviii) Tune KSURF.0 to obtain correct long channel V_t roll-off
- (xix) Use BCA model for most implants
- (xx) Measure contact resistance and add resistance to model
- (xxi) Ensure 10Å grid in inversion regions
- (xxii) Tune polygate workfunction if silicided
- (xxiii) Use quantum model for thin gate oxides
- (xxiv) Only FINE tuning for device simulation eg V_{sat} , using I-V curves surface roughness field dependent mobility (DELN.CVT) etc.
 $mobility = f*(DELN.CVT/E^2)$
- (xxv) Use alternative measured dc electrical results for confirmation eg. I-V curves with biased body contact.