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Numerical Analysis of Forward-Current/Voltage Characteristics of Vertical GaN Schottky-Barrier Diodes and p-n Diodes on Free-Standing GaN Substrates

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***Abstract*—Forward-current-density J_F/forward-voltage V_F characteristics of vertical gallium-nitride (GaN) Schottky-barrier diodes (SBDs) and p-n diodes on free-standing GaN substrates were computationally, as well as experimentally, investigated. Based on the thermionic emission model, electron-drift mobility μ_n was used as a parameter to fit the J_F–V_F characteristics of both reported and fabricated GaN SBDs. At 300 K, μ_n was fitted to be 600 $cm^2/V \cdot s$ when electron concentration n was 1×10^{16} cm^{-3} and 750 $cm^2/V \cdot s$ when n was 5×10^{15} cm^{-3}. Accordingly, the theoretical $\mu_n - n$ curve for a carrier compensation ratio of 0.90 was applied in the case of n-GaN layers on GaN substrates. With respect to GaN p-n diodes, the reported J_F–V_F characteristics were successfully fitted with dislocation-mediated carrier lifetimes in the high-injection region and with Shockley–Read–Hall lifetimes in the generation–recombination current region.**

***Index Terms*—Gallium compounds, power semiconductor devices, simulation.**

I. Introduction

GALLIUM NITRIDE (GaN) is an attractive material for optical and electronic devices, as well as sensors [1]. Its high breakdown electric field of 3.27 MV/cm [2], which is about 10% higher than that of silicon carbide (SiC) and about ten times that of silicon, makes it ideal for power devices. GaN-based power devices are usually fabricated on substrates such as sapphire, SiC, and silicon. These substrates cause dislocations in heteroepitaxially grown GaN at high density (10^8–10^{10} cm^{-2}). Free-standing GaN substrates [3]–[6] are thus expected to open the way to explore the intrinsic performance of GaN and its related alloys. Schottky-barrier diodes (SBDs) [7]–[12] and p-n diodes [2], [13], [14] have so far been fabricated on GaN substrates. To further improve the performance of these diodes, electrical characteristics of these devices should be numerically investigated. Although Shelton *et al.* [15] and Baharin *et al.* [16] simulated current–voltage characteristics of GaN SBDs and p-n diodes, the substrates that they assumed were sapphire.

In contrast to previous studies on heteroepitaxially grown GaN devices [15], [16], this paper on homoepitaxially grown GaN devices distinguishes itself in that the two parameters are carefully evaluated: drift mobility (μ_n and μ_p) and minority-carrier lifetime (τ_n and τ_p), where subscripts n and p represent electrons and holes, respectively. These parameters directly affect forward-current-density J_F/forward-voltage V_F characteristics of SBDs and p-n diodes. Among them, μ_n is known to strongly depend on carrier compensation [17], which was observed in n-type GaN on GaN substrates when net doping concentration N_D^{net} was below 5×10^{16} cm^{-3} [10]. In the previous simulation [15], however, these parameters were tentatively chosen as $\mu_n = 350$ $cm^2/V \cdot s$ (electron concentration n: 5×10^{16} cm^{-3}), $\mu_p = 12$ $cm^2/V \cdot s$ (hole concentration p: 2×10^{17} cm^{-3}), and $\tau_n = \tau_p = 1$ ns.

In this paper, the J_F–V_F characteristics of GaN SBDs and p-n diodes on GaN substrates were numerically simulated in the cylindrical coordinate system. Moreover, to determine the compensation ratio for n-GaN on GaN substrates, GaN SBDs were fabricated.

The procedure for simulation and fabrication of GaN SBDs on GaN substrates is explained in Section II. Reported [10] and measured J_F–V_F characteristics of GaN SBDs are compared with calculated J_F–V_F characteristics in Section III. The reported J_F–V_F characteristics of GaN p-n diodes [2], [14] under high- and low-injection conditions are separately investigated in Section IV. The results of this study are summarized in Section V.

II. Simulation and Fabrication of SBDs

GaN SBDs on GaN substrates were simulated in the cylindrical coordinate system by using the thermionic emission model in a commercial device simulator, i.e., ATLAS [18]. A schematic of the GaN SBD reported in [10] is shown as an example in Fig. 1. The epitaxial layers consist of 7-μm-thick GaN (Si: 1×10^{16} cm^{-3}) and 2-μm-thick n^+-GaN buffer. For the GaN substrate, thickness of 500 μm, n of 5×10^{18} cm^{-3},

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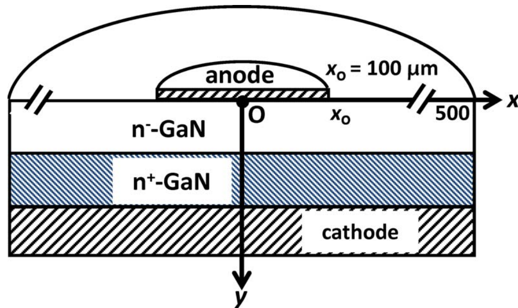

Fig. 1. Schematic of the GaN SBD on GaN substrates reported in [10].

TABLE I
MATERIAL AND ELECTRICAL PROPERTIES OF GaN USED IN THE SIMULATION

Material property	unit	value	ref.
Energy gap	eV	3.39	[27]
Relative dielectric constant		10.4	[11]
Electron effective mass	kg	$0.23\times9.1\times10^{-31}$	[11]
Hole effective mass	kg	$1.5\times9.1\times10^{-31}$	[1]
Silicon activation energy	meV	16	[1]
Magnesium activation energy	meV	175	[1]
Surface-recombination velocity	cm/s	0	

and μ_n of 170 $\text{cm}^2/\text{V}\cdot\text{s}$ [4] were assumed. Other important parameters used in the simulation are listed in Table I. For simplicity, the possible interactions between hydrogen and dopants [19] were neglected.

The GaN SBDs were fabricated by using metal–organic vapor-phase epitaxial layers grown on the Ga-polar face of a free-standing GaN substrate. The substrate was fabricated by the void-assisted separation method [6], which keeps threading-dislocation density of epitaxial layers low (around 10^6 cm^{-2}) and uniform. The epitaxial layers consist of n-type GaN ($10\ \mu\text{m}/N_D^{\text{net}} = 5\times10^{15}\ \text{cm}^{-3}$) and a 2-$\mu$m-thick n$^+$-GaN buffer. The N_D^{net} value was determined from 1-MHz capacitance–voltage measurement at room temperature. Prior to the SBD fabrication, the GaN epitaxial wafer was cleaned in an HF solution, followed by treatment in an NH_4OH solution. The epitaxial wafer was then rinsed in deionized water, dried by nitrogen gas blow, and then loaded into a vacuum-evaporation system. After forming the backside ohmic contact, which consists of conventional titanium/aluminum electrodes, 200-μm-diameter Schottky contacts were defined by evaporation of a 300-nm-thick palladium layer through a metal shadow mask.

III. SBD FORWARD ELECTRICAL CHARACTERISTICS

Fig. 2 shows the simulated J_F–V_F characteristics of the Au/n-GaN($7\ \mu\text{m}/\text{Si}: 1\times10^{16}\ \text{cm}^{-3}$) SBD reported in [10]. In the simulation, cathode contact resistance was neglected, and in Fig. 2(a), μ_n was tentatively assumed to be 600 $\text{cm}^2/\text{V}\cdot\text{s}$. As is clear in the figure, the measured results [10] were reproduced not by a reported barrier height $q\Phi_B$ of 0.88 eV for Au/n-GaN [20] but by $q\Phi_B = 1.58$ eV. This situation did not change even if μ_n was chosen to be lower than 600 $\text{cm}^2/\text{V}\cdot\text{s}$. The large discrepancy in $q\Phi_B$ might be attributable to the existence of

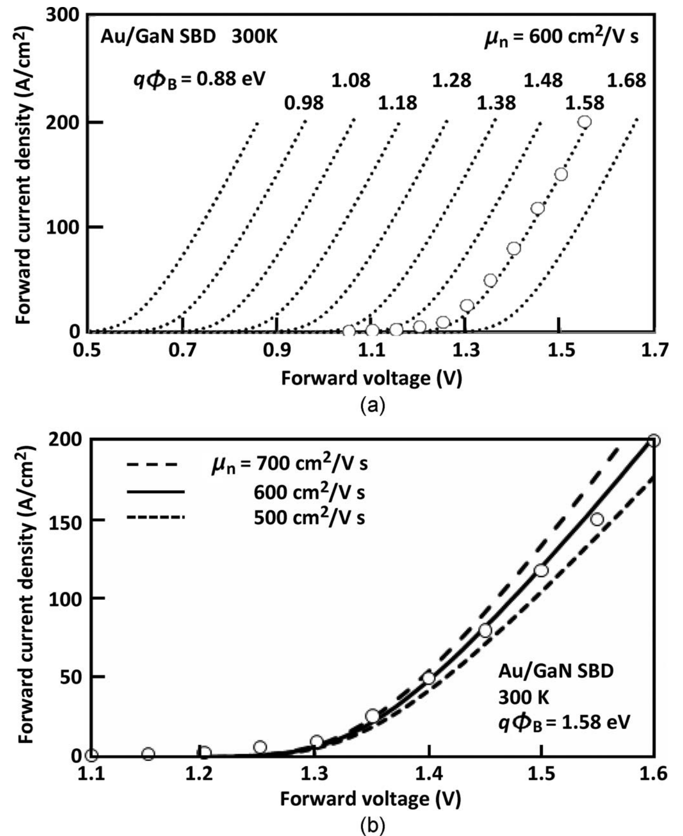

Fig. 2. (Open circles) Measured (as reported in [10]) and calculated forward-current-density/forward-voltage characteristics of the Au/n-GaN (7 μm) SBD on GaN substrates on the assumption that (a) an electron mobility is 600 $\text{cm}^2/\text{V}\cdot\text{s}$ and (b) a barrier height is 1.58 eV.

an interfacial insulator; for example, 0.16–0.23-eV increase in $q\Phi_B$ was reported for Pt–Au/n-GaN SBDs with a 1–2-nm-thick oxide layer remained at the metal–semiconductor interface [1]. The apparent $q\Phi_B$ in linear J_F–V_F plots should be increased further by the increase in the ideality factor n as follows [21]:

$$n = 1 + \{(d/\varepsilon_i)\,[(\varepsilon_s/W) + qD_{\text{sb}}]\,/\,[1 + (d/\varepsilon_i)qD_{\text{sa}}]\} \quad (1)$$

where d is the thickness, ε_i is the permittivity of the insulating layer, ε_s is the permittivity of n-GaN, W is the width of the depletion region in n-GaN, q is the elementary charge, and D_{sa} and D_{sb} are the densities of interface states (in $\text{cm}^{-2}\text{eV}^{-1}$) in equilibrium with Au and with n-GaN, respectively.

Since it is not easy to numerically simulate metal–insulator–semiconductor tunnel diodes [21], we decided to keep using the thermionic emission model, regarding $q\Phi_B$ as a fitting parameter. In Fig. 2(b), $q\Phi_B$ of 1.58 eV was thus assumed, and the three curves were calculated, with μ_n as a parameter. The measured characteristics [10], denoted by open circles, are best fitted when μ_n is 600 $\text{cm}^2/\text{V}\cdot\text{s}$.

Fig. 3 shows the simulated isocurrent-density contours of the Au/n-GaN SBD forward biased at 1.6 V. The current-conducting area is laterally spread in the GaN substrate. This finding supports the aforementioned assumption that cathode contact resistance can be neglected.

Note that an error in μ_n due to inaccuracy in determining $q\Phi_B$ remains because the reported J_F–V_F characteristics of the Au/GaN SBD are not shown in semilog plots [10]. We

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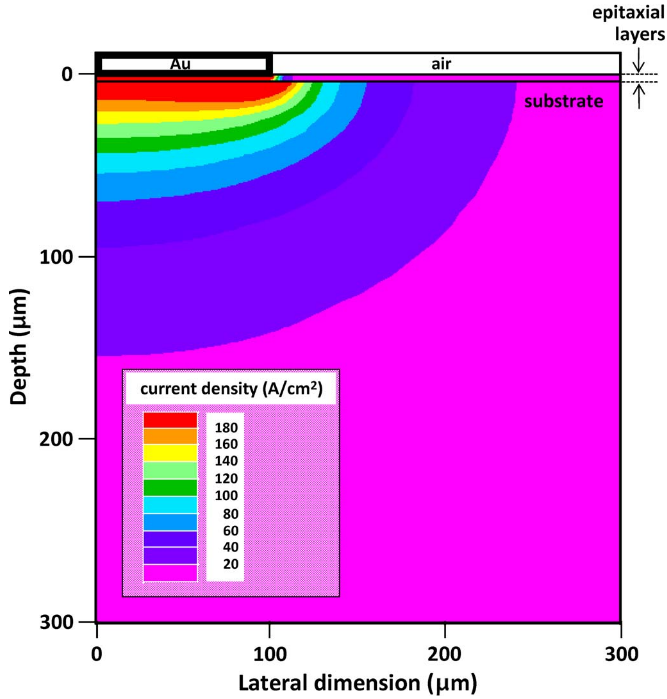
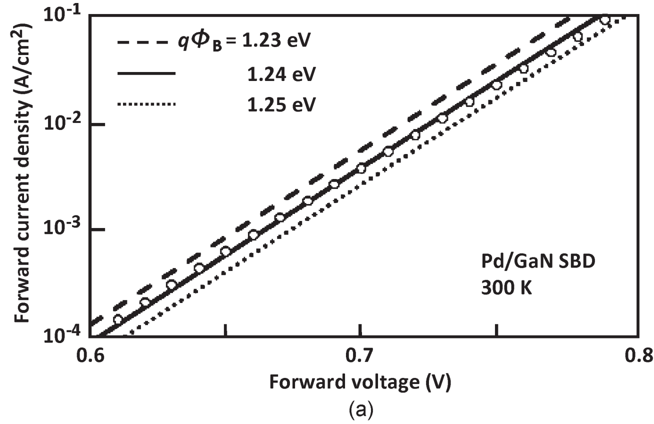


Fig. 3. Simulated isocurrent-density contours in the Au/n-GaN SBD forward biased at 1.6 V.



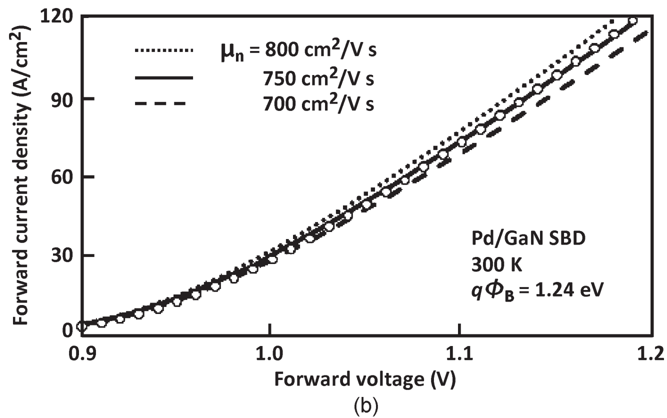


Fig. 4. Forward-current-density/forward-voltage characteristics of a Pd/n-GaN SBD on GaN substrates in (a) semilog and (b) linear plots.

thus tried to confirm the validity of the μ_n value in the case of n-GaN on GaN substrates by using the Pd/GaN SBDs described in Section II. As shown in Fig. 4(a), $q\Phi_B$ of 1.24 eV was found to best fit the measured J_F–V_F characteristics when $V_F < 0.8$ V. The use of this $q\Phi_B$ value resulted in the best fitted μ_n, namely, 750 $\mathrm{cm^2/V \cdot s}$ [see Fig. 4(b)].

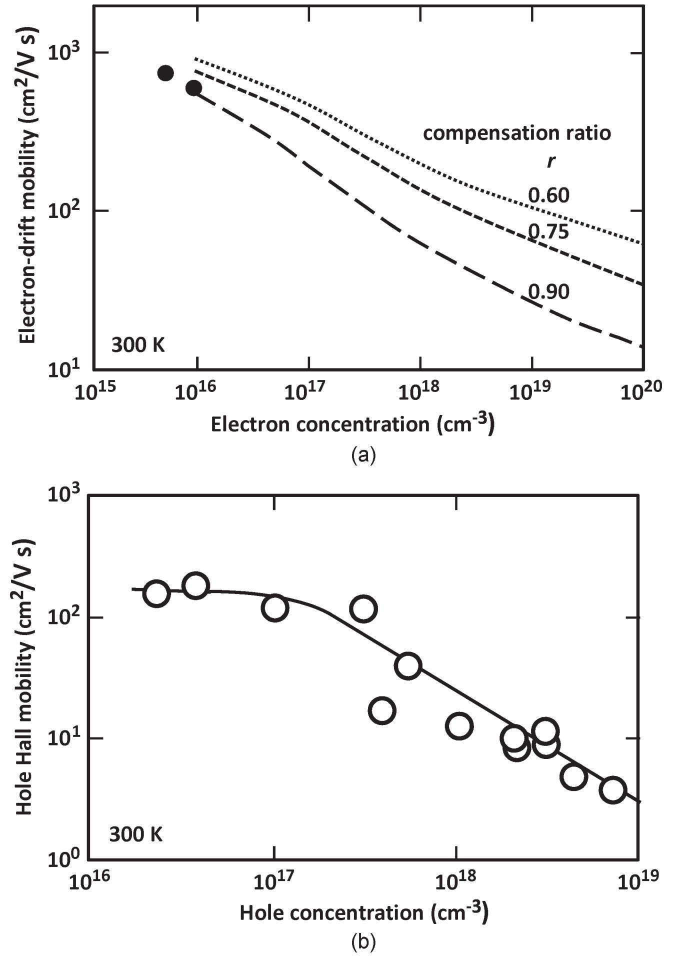


Fig. 5. Carrier-concentration dependences of (a) electron-drift mobility and (b) hole Hall mobility. The dotted and dashed lines in (a) and open symbols in (b) are taken from [17] and [27], respectively. (Solid circles) The data fitted in Figs. 2 and 4.

Some of the theoretical μ_n–n curves calculated in [17] are shown in Fig. 5(a). As shown by the solid circles, the two n-GaN layers appear to have a compensation ratio r ranging from 0.75 to 0.90. This range in r is comparable to that reported in [22] (0.7–0.85) and that in [23] (0.85); however, it is much larger than the ratio reported in [24] (0.60) and that in [25] (0.35). Although the observed carrier compensation in n-GaN on GaN substrates is probably due to residual hydrogen, oxygen, and carbon, whose concentrations were reported to be in the order of 10^{16} $\mathrm{cm^{-3}}$ [10], the carrier-compensation mechanism is still unclear. This high compensation ratio results in low μ_n but increases the dislocation-mediated electron lifetime [26], as discussed in the next section.

IV. p-n Diode Forward Electrical Characteristics

The J_F–V_F characteristics of GaN p-n diodes on GaN substrates reported in [2] and [14] are shown in Figs. 6 and 8, respectively. These diodes consist of the following epitaxial layers: $\mathrm{p^+}$-GaN ($20\ \mathrm{nm/Mg}: 2\times10^{20}\ \mathrm{cm^{-3}}$)/p-GaN ($500\ \mathrm{nm/Mg}: 2\times10^{19}\ \mathrm{cm^{-3}}$)/$\mathrm{n^-}$-GaN ($10\ \mu\mathrm{m/Si}: 2\times10^{16}\ \mathrm{cm^{-3}}$)/

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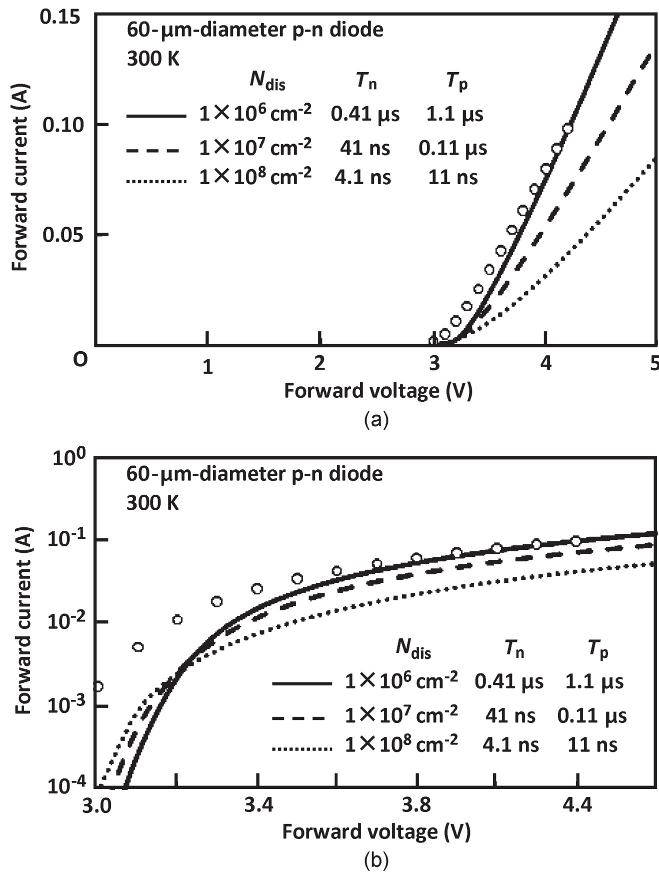

Fig. 6. (Open circles) Measured (as reported in [14]) and calculated forward-current/forward-voltage characteristics of a p-n diode on GaN substrates in (a) linear and (b) semilog plots.

n^+-GaN ($2\ \mu$m/Si:2×10^{18} cm^{-3}) [14] and p^+-GaN (75 nm)/p-GaN (500 nm/Mg : 7×10^{17} cm^{-3})/n^--GaN ($7\ \mu$m/Si : 3×10^{16} cm^{-3})/n^+-GaN (600 nm) [2]. Since the original data were presented in linear [14] and semilog plots [2], p-n diode operations under high- and low-injection conditions are separately investigated in the following.

Under high-injection condition, some of the photons created by radiative recombination are emitted from the GaN surface or absorbed within the GaN crystal. Since the mesa of p-n diodes reported in [14] was covered with spin-on glass and field-plate metal films, it is simply assumed here that all the photons are absorbed within the GaN crystal. Most of the photons would be absorbed within p^+ and n-GaN regions of the forward-biased p-n diodes, which creates electron–hole pairs. Both radiative and nonradiative recombination of the created minority carriers (i.e., electron in p^+GaN and holes in n-GaN) would then be taking place. The photons emitted through this radiative recombination would again be absorbed within the GaN crystal. Under this assumption of photon recycling effect, carrier lifetimes are considered to be limited only by nonradiative recombination.

A number of acceptorlike levels are known to be formed in GaN through threading dislocations. For dislocation-mediated lifetimes, Karpov and Makarov derived the following [26]:

$$\tau_n = (4\pi D_n N_{\text{dis}})^{-1}\left[(2D_n/aV_nS) - 3/2 - \ln(\pi a^2 N_{\text{dis}})\right] \quad (2)$$

$$\tau_p = (4\pi D_p N_{\text{dis}})^{-1}\left[(2D_p/aV_pS) - 3/2 - \ln(\pi a^2 N_{\text{dis}})\right] \quad (3)$$

where D_n (D_p) is the electron (hole) diffusivity, N_{dis} is the dislocation density, a is the lattice constant of hexagonal GaN, V_n (V_p) is the electron (hole) thermal velocity, and S is the fraction of electrically active sites on the dislocation core. Other possible impact of carrier leakage from dislocation or other structural defects is ignored.

In the current simulation, the theoretical μ_n–n curve for $r = 0.90$ [see Fig. 5(a)] was used. Although μ_n became 30% ($n = 2\times10^{16}$ cm^{-3}) to 36% ($n = 3\times10^{16}$ cm^{-3}) lower than μ_n for $r = 0.75$, the simulated results in Figs. 6 and 8 did not change very much as far as an order of magnitude change in N_{dis}, τ_n, and τ_p is concerned. The hole-drift mobility μ_p is represented by the curve in Fig. 5(b), which fits the reported data of hole Hall mobility [27]. It is assumed that the value of S is equal to 0.5 for gallium- or nitrogen-vacancy cores [26] and that minority-carrier mobility is the same as majority-carrier mobility (see Fig. 5) when D_n and D_p are calculated from the Einstein relation [28].

The three curves in Fig. 6 were calculated with N_{dis} as a parameter. As clear from (2) and (3), τ_n and τ_p increase with decreasing N_{dis}. When $N_{\text{dis}} = 1\times10^6$ cm^{-2}, i.e., $\tau_n = 0.41\ \mu$s and $\tau_p = 1.1\ \mu$s, the calculated curve becomes the closest to the measured results, although further experiments are required to discuss the validity of these ultralong lifetimes. The deviation of the measured data from the solid curve around $V_F = 3$ V in Fig. 6(a) is due to a nonideal diode current with an ideality factor of larger than unity, as shown in Fig. 6(b).

Fig. 7(a) shows isocurrent-density contours in the p-n diode [14] forward biased at 5 V. As reported in [16], current concentration is observed in the periphery of the p^+-GaN anode layer. This nonuniform current conduction is the reason that forward current, instead of J_F, is plotted in Fig. 6(a) and (b). Isocarrier-concentration contours at $V_F = 5$ V, shown in Fig. 7(b) and (c), clearly show that conductivity modulation occurs in the n^--GaN layer.

Nonideal diode current at low V_F in the p-n diode reported was also observed in [2] [open circles in Fig. 8(a) and (b)]. Since anode size was $400\times400\ \mu$m [2], the simulated anode diameter was chosen as either 452 μm (equivalent area) or 510 μm (equivalent perimeter). As shown by the dotted curve in Fig. 8(a), the use of the long lifetimes assumed in Figs. 6 and 7 underestimates J_F under a low-injection condition. The same lifetime was thus assumed for electrons and holes, and the reported characteristics were fitted using the 452-μm-diameter anode structure. The solid curve in Fig. 8(a) indicates that τ_n and τ_p of the p-n diode in [2] are about 0.1 ns. The deviation of the measured data from the solid curve ($V_F >$ 3 V) is considered to be due to large series resistance. No appearance of conductivity modulation in the measured results [2] is attributable to this large resistance, which is probably at the metal/p^+-GaN contact.

Fig. 8(b) shows forward current–voltage characteristics of the p-n diode simulated with different anode diameters. As shown by the dotted curve, $\tau_n = \tau_p = 0.1$ ns is too short in the case of the 510-μm-diameter anode. Three-dimensional simulation is therefore needed to accurately determine the lifetime in p-n diodes with a noncircular anode.

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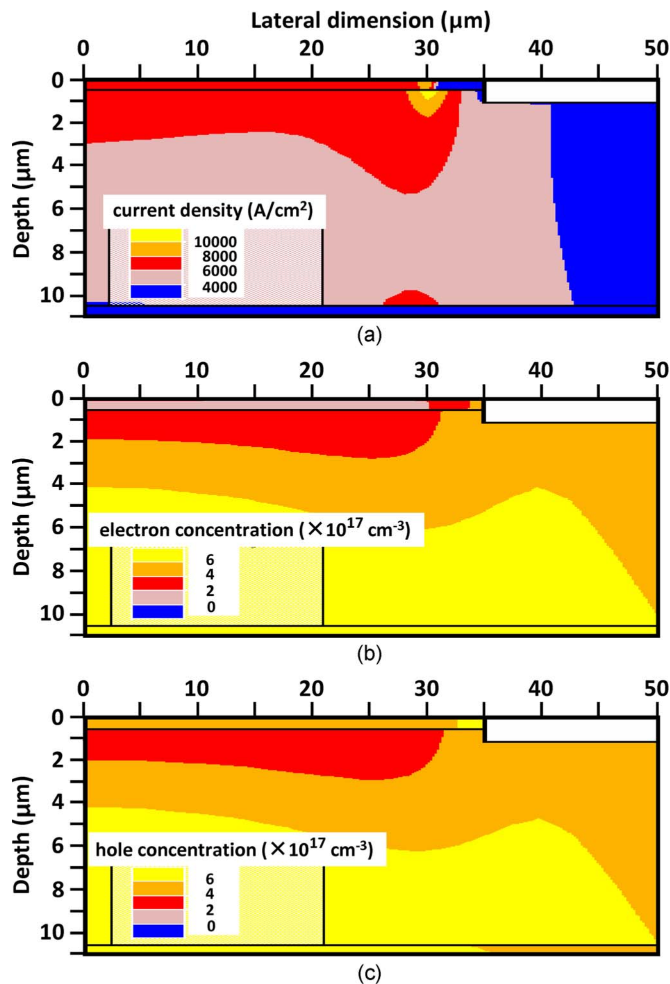

Fig. 7. Calculated contours of (a) isocurrent density, (b) isoelectron concentration, and (c) isohole concentration in a p-n diode (see Fig. 6) forward biased at 5 V.

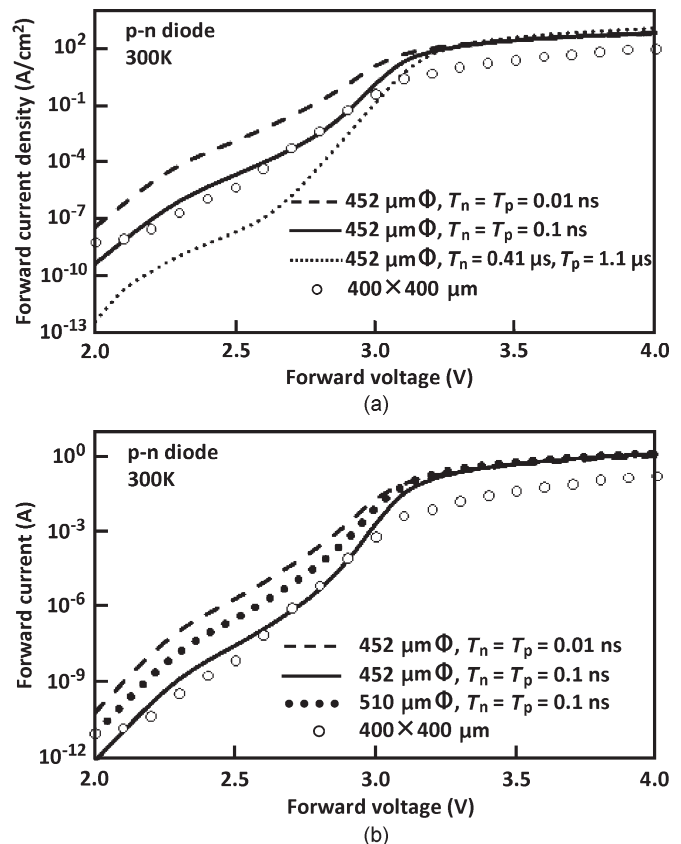

Fig. 8. (Open circles) Measured (as reported in [2]) and calculated (a) forward-current-density/forward-voltage and (b) forward-current/forward-voltage characteristics of a p-n diode on GaN substrates.

The minority-carrier lifetime is known to depend on injection level [29]. If the minority-carrier lifetime under high- and low-injection conditions is denoted by τ_H and τ_L, respectively

$$\tau_H \gg \tau_L \tag{4}$$

should be satisfied [29]. Under a low-injection condition, the influence of carrier recombination within the depletion region extending around the p-n junction is large (i.e., nonradiative recombination lifetime $\tau_{\rm NR} \approx \tau_L$). Under a high-injection condition, on the other hand, the influence of carrier recombination within the minimized depletion region becomes small (i.e., $\tau_{\rm NR} \approx \tau_H$). This supposition explains why the different carrier lifetimes were needed to fit the measured characteristics in Figs. 6 and 8.

It is finally noted that the surface-recombination velocity assumed in the simulation previously described was zero (see Table I). The quantitative agreement between the measured and calculated forward electrical characteristics in Figs. 6 and 8 indicates that surface recombination can be negligibly small in p-n diodes, even with a reactive-ion-etched mesa structure [2], [14].

V. Conclusion

Forward current–voltage characteristics of vertical GaN SBDs and p-n diodes on GaN substrates have been numerically analyzed. The characteristics of SBDs with $n = 1 \times 10^{16}$ and 5×10^{15} cm^{-3} were best fitted with $\mu_n = 600$ and $750\ \mathrm{cm^2/V \cdot s}$, respectively. Accordingly, the theoretical $\mu_n{-}n$ curve for a compensation ratio of 0.90 was applied in the case of n-GaN layers on GaN substrates. Two reported characteristics of p-n diodes were reproduced through two parameters: dislocation-mediated carrier lifetime under a high-injection condition and Shockley–Read–Hall lifetime under a low-injection condition.

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References

[1] S. J. Pearton, C. R. Abernathy, and F. Ren, *Gallium Nitride Processing for Electronics, Sensors and Spintronis*. London, U.K.: Springer-Verlag, 2006, pp. 49, 182–184.

[2] Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, "High-breakdown-voltage pn-junction diodes on GaN substrates," *J. Cryst. Growth*, vol. 298, pp. 875–878, Jan. 2007.

[3] S. S. Park, I. W. Park, and S. H. Choh, "Free-standing GaN substrates by hydride vapor phase epitaxy," *Jpn. J. Appl. Phys.*, vol. 39, no. 11B, pp. L1 141–L1 142, Nov. 2000.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[4] K. Motoki, T. Okahisa, N. Matsumoto, M. Matsushima, H. Kimura, H. Kasai, K. Takemoto, K. Uematsu, T. Hirano, M. Nakayama, S. Nakahata, M. Ueno, D. Hara, Y. Kumagai, A. Koukitsu, and H. Seki, "Preparation of large freestanding GaN substrates by hydride vapor phase epitaxy using GaAs as a starting substrate," *Jpn. J. Appl. Phys.*, vol. 40, no. 2B, pp. L140–L143, Feb. 2001.

[5] T. Paskova, D. A. Hanser, and K. R. Evans, "GaN substrates for III-nitride devices," *Proc. IEEE*, vol. 98, no. 7, pp. 1324–1338, Jul. 2010.

[6] T. Yoshida, Y. Oshima, T. Eri, K. Ikeda, S. Yamamoto, K. Watanabe, M. Shibata, and T. Mishima, "Fabrication of 3-in GaN substrates by hydride vapor phase epitaxy using void-assisted separation method," *J. Cryst. Growth*, vol. 310, no. 1, pp. 5–7, Jan. 2008.

[7] Z. Z. Bandic, P. M. Bridger, E. C. Piqette, T. C. McGill, R. P. Vaudo, V. M. Phanse, and J. M. Redwing, "High voltage (450 V) GaN Schottky rectifiers," *Appl. Phys. Lett.*, vol. 74, no. 9, pp. 1266–1268, Mar. 1999.

[8] A. P. Zhang, J. W. Johnson, B. Luo, F. Ren, S. J. Pearton, S. S. Park, Y. J. Park, and J.-I. Chyi, "Vertical and lateral GaN rectifiers on free-standing GaN substrates," *Appl. Phys. Lett.*, vol. 79, no. 10, pp. 1555–1557, Sep. 2001.

[9] J. W. Johnson, A. P. Zhang, W.-B. Luo, F. Ren, S. J. Pearton, S. S. Park, Y. J. Park, and J.-I. Chyi, "Breakdown voltage and reverse recovery characteristics of free-standing GaN Schottky rectifiers," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 32–36, Jan. 2002.

[10] S. Hashimoto, Y. Yoshizumi, T. Tanabe, and M. Kiyama, "High-purity GaN epitaxial layers for power devices on low-dislocation-density GaN substrates," *J. Cryst. Growth*, vol. 298, pp. 871–874, Jan. 2007.

[11] J. Suda, K. Yamaji, Y. Hatashi, T. Kimoto, K. Shimoyama, H. Namita, and S. Nagao, "Nearly ideal current-voltage characteristics of Schottky barrier diodes formed on hydride-vapor-phase-epitaxy-grown GaN free-standing substrates," *Appl. Phys. Express*, vol. 3, no. 10, p. 101 003, Oct. 2010.

[12] K. Mochizuki, A. Terano, N. Kaneda, T. Mishima, T. Ishigaki, and T. Tsuchiya, "Analysis of leakage current at Pd/AlGaN Schottky barriers formed on GaN free-standing substrates," *Appl. Phys. Express*, vol. 4, no. 2, p. 024 104, Feb. 2011.

[13] J. B. Lim, D. Yoo, J.-H. Ryou, W. Lee, S.-C. Shen, and R. D. Dupui, "High performance GaN pin rectifiers grown on free-standing GaN substrates," *Electron. Lett.*, vol. 42, no. 22, pp. 1313–1314, Oct. 2006.

[14] K. Nomoto, Y. Hatakeyama, H. Katayose, N. Kaneda, T. Mishima, and T. Nakamura, "Over 1.0 kV GaN p-n junction diodes on free-standing GaN substrates," in *Proc. Int. Workshop Nitride Semicond.*, Tampa, FL, Sep. 2010, to be published.

[15] B. S. Shelton, T. G. Zhu, D. J. H. Lambert, and R. D. Dupui, "Simulation of the electrical characteristics of high-voltage mesa and planar GaN Schottky and p-i-n rectifiers," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1498–1520, Aug. 2001.

[16] A. Baharin, M. Kocan, G. A. Umana-Membreno, U. K. Mishra, G. Parish, and B. D. Nener, "Experimental and numerical investigation of the electrical characteristics of vertical n-p junction diodes created by Si implantation into p-GaN," in *Proc. Conf. Optoelectron. Microelectron. Mater. Devices*, 2008, pp. 12–15.

[17] V. W. Chin, T. L. Tansley, and T. Osotchan, "Electron mobilities in gallium, indium, and aluminum nitrides," *J. Appl. Phys.*, vol. 75, no. 11, pp. 7365–7372, Jun. 1994.

[18] [Online]. Available: http://www.silvaco.com/products/device_simulation/atlas.html

[19] J. Neugebauer and C. G. Van de Walle, "Role of hydrogen in doping of GaN," *Appl. Phys. Lett.*, vol. 68, no. 13, pp. 1829–1831, Mar. 1996.

[20] A. C. Schmitz, A. T. Ping, M. Asif Khan, Q. Chen, J. W. Yang, and I. Adesida, "Schottky barrier properties of various metals on n-type GaN," *Semicond. Sci. Technol.*, vol. 11, no. 10, pp. 1464–1467, Oct. 1996.

[21] H. C. Card, "Tunneling MIS structures," *Inst. Phys. Conf. Ser.*, vol. 50, pp. 140–165, 1980.

[22] M. Ilegems and H. C. Montgomery, "Electrical properties of n-type vapor-grown gallium nitride," *J. Phys. Chem. Solids*, vol. 34, no. 5, pp. 885–895, May 1973.

[23] M. A. Khan, J. N. Kuznia, J. M. Van Hove, and D. T. Olson, "Growth of high optical and electrical quality GaN layers using low-pressure metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 58, no. 5, pp. 526–527, Feb. 1991.

[24] I. Akasaki, H. Amano, Y. Koide, K. Hiramatsu, and N. Sawaki, "Effects of AlN buffer layer on crystallographic structure and on electrical and optical properties of GaN and $Ga_{1-x}Al_xN$ $(0 < x \leq 0.4)$ films grown on sapphire substrate by MOVPE," *J. Cryst. Growth*, vol. 98, no. 1/2, pp. 209–219, Nov. 1989.

[25] S. Nakamura, T. Mukai, and M. Senoh, "In situ monitoring and Hall measurements of GaN grown with GaN buffer layers," *J. Appl. Phys.*, vol. 71, no. 11, pp. 5543–5549, Jun. 1992.

[26] S. Y. Karpov and Y. N. Makarov, "Dislocation effect on light emission efficiency in gallium nitride," *Appl. Phys. Lett.*, vol. 81, no. 25, pp. 4721–4723, Dec. 2002.

[27] [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/GaN/index.html

[28] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ: Wiley, 2007, p. 46.

[29] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York: Springer-Verlag, 2008, p. 62.

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